WHAT IS CLAIMED IS:

1. A semiconductor device having an actual pattern and plural types of dummy patterns on a wiring layer thereof,

wherein said plural types of dummy patterns on the wiring layer have at least either of a different size or a different shape from each other for the type of said dummy pattern.

2. The semiconductor device according to claim 1,

wherein said dummy patterns are different in size for each type.

3. The semiconductor device according to claim 1,

wherein said dummy patterns have rectangular shapes with same longer sides and different shorter sides in length, the shorter sides being different from each other for each type.

4. A semiconductor device having an actual pattern, a first dummy pattern, and a second dummy pattern on a wiring layer thereof,

wherein said second dummy pattern has at least either of a different shape or a different size from corresponding that of the first dummy pattern.

5. The semiconductor device according to claim 4,

wherein said second dummy pattern is smaller than said first dummy pattern.

6. The semiconductor device according to claim 5,

wherein said second dummy pattern has a rectangular shape.

7. The semiconductor device according to claim 5, wherein said first dummy pattern has a square shape and said second dummy pattern has a rectangular shape with same longer sides in length as one side of said first dummy pattern and shorter sides which are shorter than said one side.

8. A pattern generation method comprising:

a first dummy pattern arrangement step including arranging first dummy patterns by generating the first dummy patterns in a region allowed to generate the first dummy pattern based on a layout data having actual patterns arranged on a wiring layer in a semiconductor device; and

a repeated step including repeating a kth dummy pattern arrangement step by incrementally changing a value of k, said kth dummy pattern arrangement step including arranging kth dummy patterns by generating the kth dummy patterns being different from the first to the (k-1)th (k is a natural number from 2 to N, N is optional.) dummy patterns in a region allowed to generate the kth dummy pattern based on the layout data having actual patterns and the first to the (k-1)th dummy patterns arranged on the wiring layer.

9. The pattern generation method according to claim 8,

wherein the first dummy pattern is a biggest in size and the kth dummy patterns have sizes which are

decrementally changed along with the values of the k which are incrementally changed.

10. The pattern generation method according to claim 9,

wherein the first to the kth dummy patterns have rectangular shapes.

11. The pattern generation method according to claim 10,

wherein the first to the kth dummy patterns have same longer sides in length with each other.

12. The pattern generation method according to claim 8,

wherein each dummy pattern is arranged by rotating a corresponding angle when arranging the kth dummy pattern in the kth dummy pattern arrangement step.

13. The pattern generation method according to claim 8, wherein the first dummy pattern arrangement step comprises:

generating the dummy pattern,

judging whether or not the dummy pattern generated meets an arrangement rule; and

excluding the dummy pattern not meeting the arrangement rule, based on the judgment result.

14. A pattern generation method comprising:

a first dummy pattern arrangement step including arranging first dummy patterns by generating the first dummy patterns in a region allowed to generate

the first dummy pattern, based on a layout data having an actual pattern arranged on a wiring layer in a semiconductor device; and

a second dummy pattern arrangement step including arranging second dummy patterns by generating the second dummy patterns in a region allowed to generate the second dummy pattern based on the layout data having the actual pattern and the first dummy pattern arranged on the wiring layer, the second dummy pattern being a dummy pattern different from the first dummy pattern.

15. The pattern generation method according to claim 12,

wherein the value of the k is 2 and, in the second dummy pattern arrangement step, the second dummy pattern is arranged by rotating an angle of 0 (zero) degrees, and after that, based on a layout data having the actual pattern, the first dummy pattern, and the second dummy pattern rotated the angle of 0 (zero) degrees, which are arranged in the wiring layer, the second dummy pattern is generated and arranged by rotating the angle of no more than 90 degrees in the region allowed to generate the second dummy pattern.